

The diagram shows a power MOSFET driver circuit. On the left, a current source is formed by two NMOS transistors, V3 and V4, with their sources connected to ground (ZW) and their gates connected to a common gate voltage  $U_{ZW}$ . The drain of V3 is connected to the gate of the main power MOSFET V1a, and the drain of V4 is connected to the gate of V1b. The gates of V3 and V4 are also connected to a common gate voltage  $U_{ZW}$ . The drain of V4 is connected to the gate of V2a. The drain of V3 is connected to the gate of V2b. The gates of V1a and V1b are connected to a common gate voltage  $U_{ZW}$ . The gates of V2a and V2b are connected to a common gate voltage  $U_{ZW}$ . The drains of V1a and V1b are connected to a common drain voltage  $U_{ZW}$ . The drains of V2a and V2b are connected to a common drain voltage  $U_{ZW}$ . The gates of V1a and V1b are connected to a common gate voltage  $U_{ZW}$ . The gates of V2a and V2b are connected to a common gate voltage  $U_{ZW}$ . The drains of V1a and V1b are connected to a common drain voltage  $U_{ZW}$ . The drains of V2a and V2b are connected to a common drain voltage  $U_{ZW}$ .

FIG 2

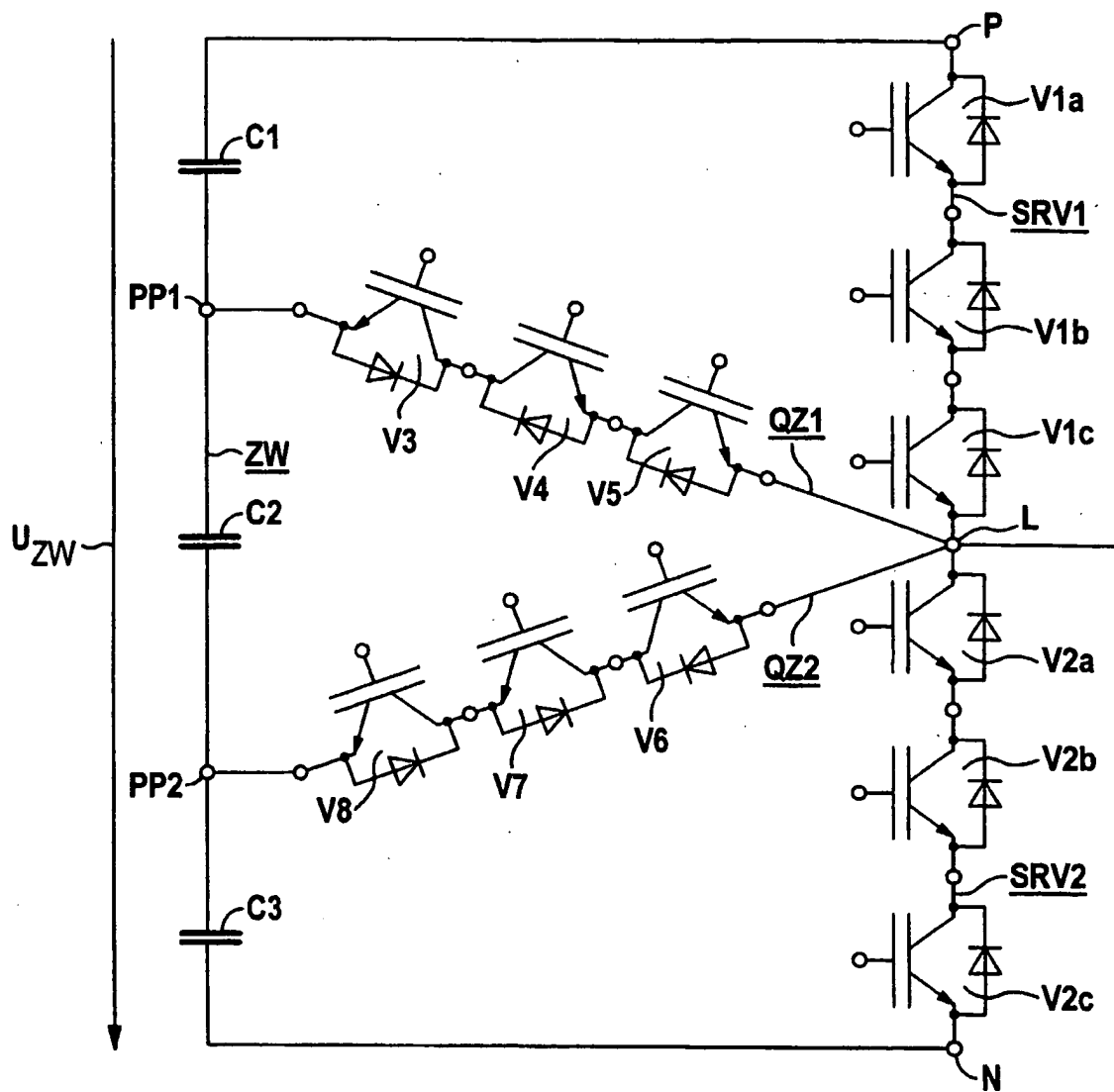


FIG 3

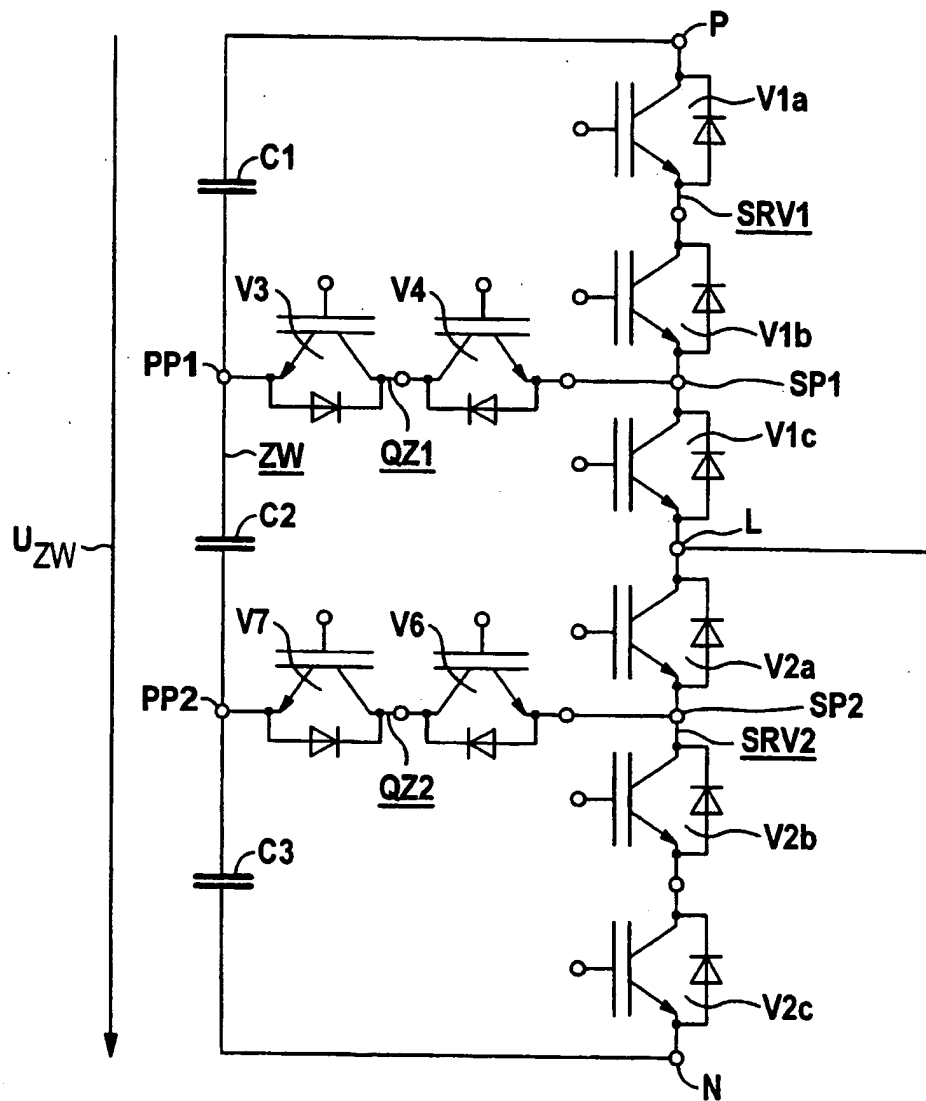


FIG 4

